WHAT IS CLAIMED IS:

1. A method of plating an integrated circuit, comprising:

positioning an activation plate adjacent to at least one integrated circuit, the integrated circuit including a plurality of bond pads comprising a bond-pad metal, and the activation plate comprising the bond-pad metal;

plating a layer of electroless nickel on the bond pads and the activation plate; and

plating a layer of gold over the layer of electroless nickel on the bond pads and the activation plate.

2. The method of claim 1 wherein the bond-pad metal comprises copper.

3. The method of claim 1 wherein the bond-pad metal comprises aluminum.

4. The method of claim 1 wherein the activation plate is positioned a distance between 0.125 inches and 0.250 inches from the at least one integrated circuit.

5. The method of claim 1 wherein the layer of electroless nickel is plated to a thickness between 0.5 microns and 5.0 microns.

6. The method of claim 1 wherein the layer of gold is plated to a thickness between 0.05 microns and 1.5 microns.

7. The method of claim 1 wherein the layer of gold is plated using one of an immersion gold or an electroless gold.

8. The method of claim 1 wherein the at least one integrated circuit is contained on a semiconductor wafer.

9. The method of claim 1 wherein the at least one integrated circuit is mounted on a carrier substrate when the layer of electroless nickel is plated.

10. The method of claim 1 further comprising:

plating a layer of electroless palladium on the plurality of bond pads and the activation plate after plating the layer of electroless nickel and prior to plating the layer of gold.

11. The method of claim 10 wherein the layer of electroless palladium is plated to a thickness between 0.2 microns and 1.0 micron.

12. The method of claim 1 further comprising:

zincating the plurality of bond pads and the activation plate prior to plating the layer of electroless nickel, the bond-pad metal comprising aluminum.

13. A system for plating an integrated circuit, comprising:

means for positioning an activation plate adjacent to at least one integrated circuit, the integrated circuit including a plurality of bond pads comprising a bond-pad metal, and the activation plate comprising the bond-pad metal;

means for plating a layer of electroless nickel on the bond pads and the activation plate; and

means for plating a layer of gold over the layer of electroless nickel on the bond pads and the activation plate.

14. The system of claim 13 wherein the activation plate is positioned a distance between 0.125 inches and 0.250 inches from the at least one integrated circuit.

15. The system of claim 13 further comprising:

means for plating a layer of electroless palladium on the bond pads and the activation plate after plating the layer of electroless nickel and prior to plating the layer of gold.

16. The system of claim 13 further comprising:

means for zincating the plurality of bond pads and the activation plate prior to plating the layer of electroless nickel, the bond-pad metal comprising aluminum.

17. An integrated circuit, comprising:

a plurality of bond pads comprising a bond-pad metal;

a layer of electroless nickel plated on the bond pads, wherein an activation plate comprising the bond-pad metal is positioned adjacent to the integrated circuit when the layer of electroless nickel is plated on the bond pads; and

a layer of gold plated over the layer of electroless nickel, wherein the activation plate is positioned adjacent to the integrated circuit when the layer of gold is plated on the nickel-plated bond pads.

18. The integrated circuit of claim 17 wherein the bond-pad metal comprises one of copper or aluminum.

19. The integrated circuit of claim 17 wherein the plated layer of gold comprises one of an electroless gold or an immersion gold.

20. The integrated circuit of claim 17 wherein the layer of electroless nickel is plated to a thickness between 0.5 microns and 5.0 microns.

21. The integrated circuit of claim 17 wherein the layer of gold is plated to a thickness between 0.05 microns and 1.5 microns.

22. The integrated circuit of claim 17 further comprising:

a layer of electroless palladium positioned between the layer of electroless nickel and the layer of gold.

23. The integrated circuit of claim 22 wherein the layer of electroless palladium is plated to a thickness between 0.2 microns and 1.0 micron.

24. The integrated circuit of claim 17 further comprising:

a layer of zinc positioned between the bond pads and the layer of electroless nickel when the bond-pad metal comprises aluminum.

25. The integrated circuit of claim 17 wherein the integrated circuit with the plurality of bond pads is contained on a semiconductor wafer.